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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
JP920020166US1	10/605,292
Applicant(s) KOHJI HOSOKAWA, ET AL.	
Filing Date 9/19/03	**Group Art Unit**

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
MT		07-094597	07.04.95	JAPAN				
		2001-168300	22.06.01	JAPAN				
		02-183489	18.07.90	JAPAN				
MT		04-094569	26.03.92	JAPAN				

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

MT		Article: IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 6, JUNE 1999 "MULTIPLE TWISTED DATALINE TECHNIQUES FOR MULTIGIGABIT DRAMS'S" , by Dong-Sun Min, pp. 856-865
MT		Article in ISSCC 2002 Digest of Technical Papers, Sessin 9, 9.3 "A 300MHz Multi-banked eDRAM Macro Featuring GND Sense, Bit-Line Twisting and Direct Reference Cell Write" by John Barth, Darren Anand, Jeff Dreibelbis, Erik Nelson pp. 156-157

EXAMINER	M. TRAN	DATE CONSIDERED	10/26/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.